

What is claimed here is:

1. A low-power-loss power semiconductor switching device comprising an n-type base, a backside p<sup>+</sup> emitter and a general frontside structure including a cathode and a gate, wherein said switching device includes a combination of an ultra-thin and lightly-doped backside p<sup>+</sup> emitter formed by ion implanting and a nonuniformly doped n-type base which contains a residual layer of a priorly-diffused n<sup>+</sup> layer on one side of the device.

2. The switching device as defined in claim 1 wherein the thickness of the backside p<sup>+</sup> emitter is approximately between 0.2 and 1 μm.

3. The switching device as defined in claim 1 wherein the implanting dose of the backside p<sup>+</sup> emitter is approximately between  $1 \times 10^{11}$  and  $1 \times 10^{17}$  cm<sup>-2</sup>.

4. The switching device as defined in claim 1 wherein the thickness of the n-type residual diffused-layer contained in the n-type base is approximately between 5 and 50 μm.

5. The switching device as defined in claim 1 wherein the doping concentration of the n-type residual diffused-layer is in a range of approximately  $1 \times 10^{14} \sim 1 \times 10^{17}$  cm<sup>-3</sup> at the interface of the residual layer and the backside p<sup>+</sup> emitter

6. A method for fabricating low-power-loss power semiconductor switching device, wherein the fabrication is in the following sequence:

PROCEDURE I: fabricating a nonuniformly doped n-type substrate which contains a diffused n<sup>+</sup> layer on one side, wherein the diffused layer, which is finally near to the backside p<sup>+</sup> emitter, is formed in the first step of this procedure before the thinning of the substrate;

PROCEDURE II: fabricating the general frontside structure of either an IGBT, MCT, or GTO on the low-concentration side of the n-type substrate using ion implanting, high-temperature diffusion and so on;

PROCEDURE III: thinning the wafer from the high-concentration side of the substrate by such commonly used techniques as grinding and polishing, so that the thickness of the residual diffused-layer is decreased to a required value;

PROCEDURE IV: forming the backside p<sup>+</sup> emitter with a required thickness by ion implanting into the surface of the residual diffused-layer;

PROCEDURE V: depositing metals on the surface of the backside p<sup>+</sup> layer, followed by sintering/alloying; and  
after the substrate is thinned, i.e. after PROCEDURE III or since PROCEDURE IV, only low-temperature processes occur.

5        7. The method as defined in claim 6, wherein said low temperature is considered to be less than 600 °C.

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